REMARKS

The Examiner is thanked for his Office Action.

The claims presently outstanding are Claims 1-46. By the foregoing amendments, various Claims are sought to be amended or cancelled without prejudice. These changes are believed not to introduce new matter, and their entry is respectfully requested.

Art Rejections

The art rejections are all respectfully traversed. Claims 1-46 were rejected over Rossin et al. (US patent 5,877,773) in view of Watkins (US patent 5,361,386) and further in view of Narayanaswami (US patent 5,613,052).

Review of the References

Some of the major technical differences between the references applied and the disclosure of the present application will now be reviewed. Of course, these points in the specification do not define the scope or interpretation of any of the claims; they are listed merely to help appreciate the importance of the claim distinctions which will be reviewed thereafter.

Rossin et al. appears to disclose the use of a VRAM and a VLUT (vertex look up table) to store vertex data and vertex indices. Specifically, Rossin shows a VRAM holding vertices and a VLUT holding indices that point to the corresponding vertex data location in the VRAM. Rossin does not appear to teach the use of circular buffers to store polygon data.

Watkins et al. appears to disclose using relational coordinates for polygon calculations. Watkins does not appear to teach the use of circular buffers.

Narayanaswami appears to disclose a method for clipping a graphical polygon to a clip region. Narayanaswami does not appear to

teach the use of circular buffers.

If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out very specifically where such teaching may be found.

Analysis of Examiner's Rejection

In view of this analysis, it may be seen that there are some significant problems with the Examiner's carefully stated arguments.

Rossin et al. does not show the use of circular buffers to store data, but rather shows only the use of two separate, non-circular buffers. **Figures 5A and 5B** from Rossin (discussed at col. 11, ll. 21-67 and col. 12, and col. 13) show the working of the VRAM and the VLUT. Unlike a circular buffer, where stored data is operated on sequentially, the VRAM and VLUT of Rossin allow exchanges of data anywhere in the VRAM, and the VLUT is used to index those changes (see col. 11, ll. 66-67, col. 12, ll. 1-3). This is contrary to the use of circular buffers as described in the specification of the present application (see, for example, p. 62, ll. 21-29, p. 63, ll. 1-7; see also **Figure 8**). The specification of the present application specifically distinguishes the VRAM and VLUT architecture shown in Rossin at p. 62, ll. 21-23 ("The input and output clipped polygons are stored in a circular buffer rather than two separate buffers which are ping-ponged between as this takes up much less storage) from the circular buffers used in the present application.

Using the circular buffer, and the sequential processing that it allows, alleviates the need for an extra memory buffer to index polygon locations. Thus, where the Rossin reference requires both storage for the vertex data (the VRAM) and storage for the indices to locate those data (the VLUT), the circular buffer taught in the present application requires only one buffer.

Analysis of Claim Amendments

Claims 16 and 19 were amended to include information consistent

with the disclosure. Claims 36 and 43 were amended to include their respective independent claims. Claims 29-35, 37-42, and 44-46 were amended to change the claims from which they depend. No new matter is believed to be added, and their entry is respectfully requested.

Claim Distinctions

Some features of the claims are noted as follows for the Examiner's convenience, but of course these notes do not dictate the interpretation of the claim, nor indicate that some features are more important than others.

None of the references relied on, singly or in any motivated combination, are seen to teach or suggest the claimed features of: "using a clipping algorithm with a circular buffer to store input and output polygons," as recited, with other limitations, in the context of Claim 1.

None of the references relied on, singly or in any motivated combination, are seen to teach or suggest the claimed features of: "circuitry to implement a clipping algorithm with a circular buffer to store input and output polygons," as recited, with other limitations, in the context of Claim 16.

None of the references relied on, singly or in any motivated combination, are seen to teach or suggest the claimed features of: "wherein two circular buffers are used to store said input and output polygons," as recited, with other limitations, in the context of Claim 36 as amended.

None of the references relied on, singly or in any motivated combination, are seen to teach or suggest the claimed features of: "wherein two circular buffers are used to store said input and output polygons," as recited, with other limitations, in the context of Claim 43 as amended.

Conclusion

Thus, all grounds of rejection and/or objection are traversed or accommodated, and favorable reconsideration and allowance are respectfully requested. The Examiner is requested to telephone the undersigned attorney or agent for an interview to resolve any remaining issues.

Respectfully submitted,

Patrick Holmes, Reg.No. 46,380
Attorney for Applicant
17000 Preston Rd. #230, Dallas TX 75248
(972) 380-6333

September 21, 2000